NEC

MOS FIELD EFFECT TRANSISTOR

2SK3480

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3480 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

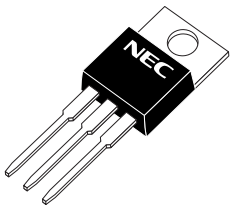
- Super low on-state resistance:
  $R_{DS(on)1}$ = 29 mΩ MAX. (V_{GS} = 10 V, I_D = 25 A)
  $R_{DS(on)2}$ = 34 mΩ MAX. (V_{GS} = 4.5 V, I_D = 25 A)
- Low C_{iss}: C_{iss} = 3600 pF TYP.
- Built-in gate protection diode

ORDERING INFORMATION

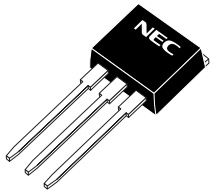
PART NUMBER	PACKAGE
2SK3480	TO-220AB
2SK3480-S	TO-262
2SK3480-ZJ	TO-263
2SK3480-Z	TO-220SMD[Note]

Note TO-220SMD package is produced only in Japan.

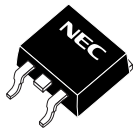
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±50	A
Drain Current (pulse) [Note1]	$I_{D(pulse)}$	±200	A
Total Power Dissipation (T_C = 25°C)	P_T	84	W
Total Power Dissipation (T_A = 25°C)	P_T	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current [Note2]	I_{AS}	T.B.D. [Note3]	A
Single Avalanche Energy [Note2]	E_{AS}	T.B.D. [Note3]	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

3. T.B.D. :To be determined

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.48	°C/W
Channel to Ambient	$R_{th(ch-A)}$	83.3	°C/W

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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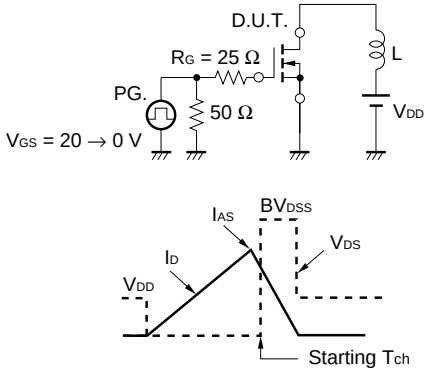
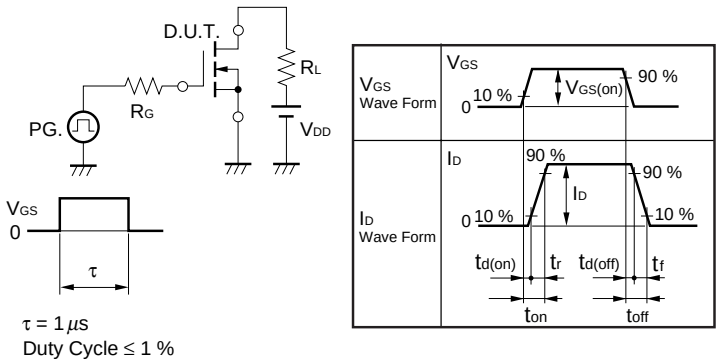
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 25 A		23	29	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 25 A		25	34	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 25 A	20	40		S
Drain Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		3600		pF
Output Capacitance	C_{oss}			360		pF
Reverse Transfer Capacitance	C_{rss}			180		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 25 A, $V_{GS(on)}$ = 10 V, V_{DD} = 50 V,		20		ns
Rise Time	t_r	R_G = 1 Ω		10		ns
Turn-off Delay Time	$t_{d(off)}$			60		ns
Fall Time	t_f			10		ns
Total Gate Charge	Q_G	I_D = 50 A , V_{DD} = 80 V, V_{GS} = 10 V		65		nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			18		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 50 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 50 A, V_{GS} = 0 V,		88		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		170		nC

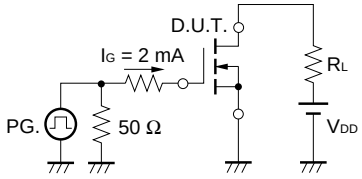
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

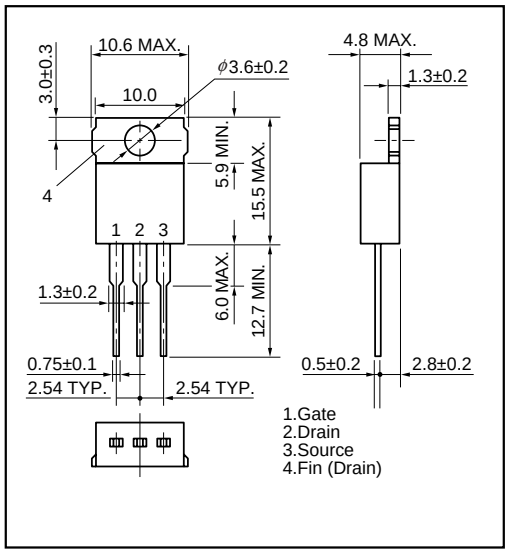


TEST CIRCUIT 3 GATE CHARGE

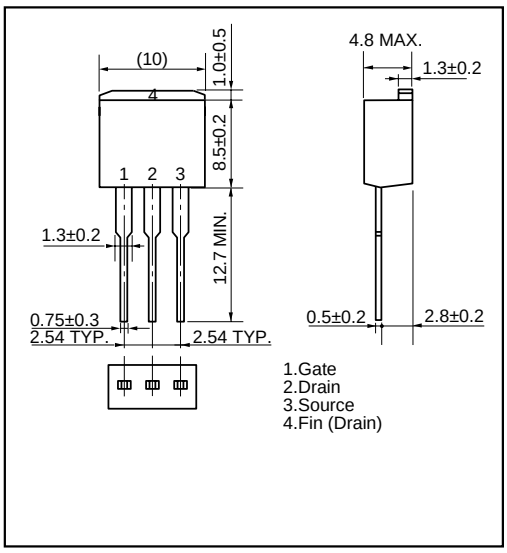


PACKAGE DRAWINGS (Unit: mm)

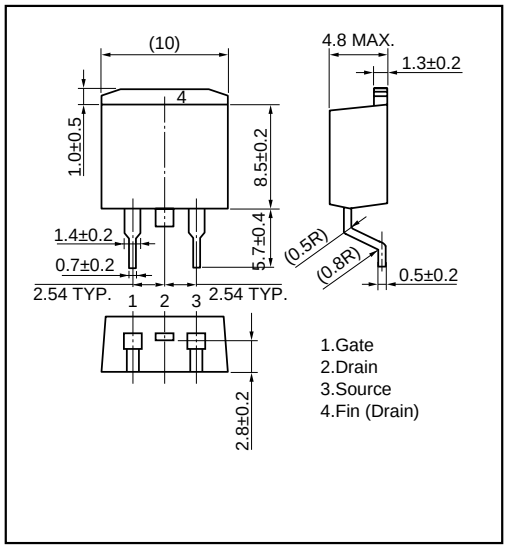
1) TO-220AB(MP-25)



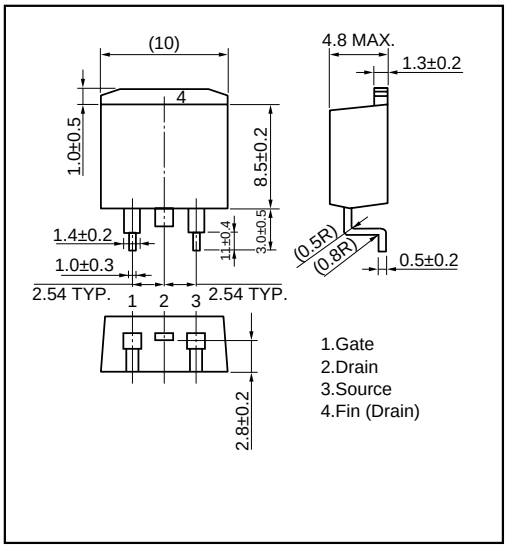
2) TO-262(MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)

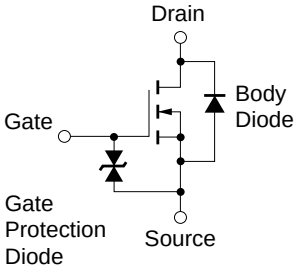


4) TO-220SMD(MP-25Z)[Note]



Note This Package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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